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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09,316,697	05/21/1999	HONGYONG ZHANG	07977/103002	8187

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EXAMINER
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QI, ZHI QIANG

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/316,697

Applicant(s)

ZHANG, HONGYONG

Examiner

Mike Qi

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,33-36,54-58 and 77-95 is/are pending in the application.
- 4a) Of the above claim(s) 77-90 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,33-36,54-58 and 91-95 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/768,066.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 20.

- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Art Unit: 2871

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the drawings must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The claims 1, 54 and 91 claimed that "a first plurality of conductive layers interposed between said first substrate and said sealing member, . . . ; a second plurality of conductive layers interposed between said first substrate and said sealing member, . . . ; a second insulating film disposed between said first plurality of conductive layers and said second plurality of conductive layers wherein said second insulating film comprises a same material as said first insulating film, . . ." in which the first plurality of conductive layers and the second plurality of conductive layers cannot be found in the drawings which layers are the first plurality of conductive layers and which layers are the second conductive layers, and the second insulating film can be any insulating film which is also cannot be found in the drawings.

### ***Claim Objections***

2. Claims 1, 54 and 91 are objected to because of the following informalities:

Art Unit: 2871

Claims 1, 54 and 91, the first plurality of conductive layers and the second plurality of conductive layers can be any conductive layers, and the second insulating film can be any insulating film, because they cannot be found according to the drawings, even they cannot be found the definitions in the specification. Therefore, for examination purpose, they are interpreted as any dummy electrode would be the first and second plurality of conductive layers and the insulating gap functions as an insulation.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 33-36, 54-58 and 91-95 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,200,847 (Mawatari et al) in view of US 5,619,358 (Tanaka et al) and JP 6-51332.

Claims 1, 54 and 91, Mawatari discloses (col. 5, line 55 - col. 8, line 55 and Figs. 3,4,6) a structure of a liquid crystal display comprising:

- a pair of substrates (101, 102) opposed to each other;
- a plurality of scanning lines (104) extending over the first substrate (101) in x direction (a first direction);

Application/Control Number: 09/316,697

Art Unit: 2871

- a plurality of data lines (105) (signal lines) extending over the first substrate (101) in Y direction (a second direction);
- a plurality of thin film transistor (TFT 106) disposed at each intersection of the scanning lines (103) and the data lines (105);
- a plurality of pixel electrodes (107) electrically connected to the thin film transistors (TFT 106);
- a gate insulating film (109) (a first insulating film) disposed between the scanning lines (104) and the signal lines (105), because the gate insulating film (109) covering the scanning line (104) and the data line (105) (signal line) is arranged on the gate insulating film (109) (col.6, lines 9-10, 20-21);
- a sealing member (103) disposed at a periphery of the substrates (101, 102);  
(concerning claim 54)
- a driver circuit (120, 121) comprising driver elements (118, 119) including many thin-film transistors (120a, 121a) (at least one half thin film transistor) formed over the first substrate (101) and disposed within a region surrounded by the sealing member (103).

Mawatari does not expressly disclose that a first and a second plurality of conductive layers interposed between the first substrate and the sealing member, the first conductive layer comprising a same material as scanning lines, the second conductive layer comprising a same material as signal lines, and a second insulating film disposed between the first and the second conductive layers wherein the insulating film comprising a same material as the first insulating film, and the first and second conductive layers are arranged in turn and are not overlapped.

Application/Control Number: 09/316,697

Art Unit: 2871

However, Tanaka discloses (col. 4 line 50 - col.10 line 40 and Figs 1-11) that each substrate includes dummy electrodes (27a, 27b) on the liquid crystal layer side to keep the thickness of the liquid crystal layer uniform; in which the dummy electrode is composed of first and second conductive films (25, 26) and interposed between substrate (21) and sealing member (29), and are arranged in turn and are not overlapped; in which a gap is provided between the first and second conductive layers, and the second conductive film is electrically isolated from the first conductive film.

Tanaka discloses (col.5, lines 9-14) that the second conductive film does not have any portion electrically connected with the first conductive film and display electrode, so that an electrolytic corrosion generated in the second conductive film is prevented from propagating into the first conductive film and display electrode through electrically connected portion.

Tanaka also indicated (col.5, lines 20-24) that since the first and second conductive films are disposed in the contacting region, so that the thickness of the liquid crystal layer near the sealing member is uniform.

Tanaka also indicated (col.5, lines 47-50) that owing to thus arranged dummy electrodes, the thickness of the liquid crystal layer near the sealing member is uniform, and the display quality is enhanced.

JP 6-51332 also discloses (Figs.1-2) using upper dummy electrode (5) and lower dummy electrode (6) at the peripheral part of the screen to eliminate the thickness difference so as to eliminate the color irregularity.

Art Unit: 2871

Concerning the material of the first conductive layer is a same material as scanning lines and the material of the second conductive layer is a same material as signal lines were common and known in the art as the conductive properties using same conductive material would simplify the manufacture process. Because the material of the scanning lines and the signal lines must be conductive material. The invention is to make the sealing material uniform. Using same material would be easier for the manufacture process and the same material would have same property to keep the sealing material uniform, since the conductive layers extend the same direction as the scanning lines and the signal lines, and that would have been at least obvious. Concerning using same material as the material of the insulating films were common and known in the art as the electrically isolating property and simplify the manufacture process.

Therefore, it would have been obvious to arrange such first and second conductive layers between the substrate and sealing member for achieving the liquid crystal layer having uniform thickness.

Therefore, it would have been obvious to use same materials for the conductive layers and use the same material for the insulating layers for achieving simplify the manufacture process.

Therefore, it would have been obvious to arrange the second conductive film do not overlap the first conductive layer for preventing the electrolytic corrosion.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange such first and second conductive layers as claimed in claims 1, 54 and 91

Application/Control Number: 09/316,697

Art Unit: 2871

for achieving uniform thickness, simplify the manufacture process, preventing the electrolytic corrosion and enhancing the display quality.

Claims 33, 55 and 92, the thin film transistors using top-gate type or bottom-type were conventional depending on the different applications and that would have been at least an obvious variations.

Claims 34, 56 and 93, the channel region of the thin film transistor using crystalline structure were conventional as the crystalline silicon film would have a high speed for the driving operation, and that would have been at least an obvious variations.

Claims 35-36, 57-58 and 94-95, Tanaka discloses (col.5, lines 6-23) that the second conductive film does not have any portion electrically connected with the first conductive film and display electrode (such as the scanning lines and signal lines), i.e., electrically isolated, so that an electrolytic corrosion generated in the second conductive film is prevented. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the first and second conductive layers isolated from the scanning lines and the signal lines for preventing the electrolytic corrosion.

### ***Response to Arguments***

6. Applicant's arguments filed on Mar. 24, 2003 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:



Art Unit: 2871

1) The reference Tanaka's conductive layers are different from the claimed layers and Tanaka does not teach an insulating film between the first and second conductive films.

2) The references do not disclose the first conductive layer to be formed of a same material as the scanning lines and the second conductive layer to be formed of the same material as the signal lines.

3) The references do not disclose that both the first and second plurality of conductive layers are formed between the first substrate and the sealing member.

Examiner's responses to applicant's **only** arguments are as follows:

1) As the claim objections indicted that the first and second conductive layers cannot be found according to the drawings, so that the first and second conductive layers can be any conductive layers between the substrate and the sealing member. The reference Tanaka discloses (col.5, lines 9-14) that the second conductive film does not have any portion electrically connected with the first conductive film and display electrode, in which a gap is provided between the first and second conductive layers and functions as an insulation, and the second conductive film is electrically isolated from the first conductive film.

2) Even though the references do not disclose using same material as claimed, but the material of the scanning lines and the signal lines must be conductive material. Using same material would be easier for the manufacture process and the same material would have same property to keep the sealing material uniform, and that would have been at least obvious.

3) The reference Tanaka discloses (col. 4 line 50 - col.10 line 40 and Figs 1-11) that the dummy electrode is composed of first and second conductive films (25, 26) and interposed

Application/Control Number: 09/316,697

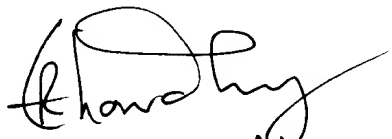
Art Unit: 2871

between substrate (21) and sealing member (29). i.e., both the first and second plurality of conductive layers are formed between the first substrate and the sealing member.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703)308-6213 .

Mike Qi  
Apr. 25, 2003

  
T. Chandhury  
Primary Examiner